CLAIMS:

1. A transceiver for a serial data bus, in which the transceiver is connected via a transmission line (TXD) and a receiving line (RXD) to a protocol controller, which manages a data bus protocol and which is coupled to the lines (2, 3) of the data bus, and in which the transceiver comprises means (1) for error management which supply an error signal (F) when they recognize that the data bus lines (2, 3) are active and when the receiving line (RXD) simultaneously signalizes an inactive bus, said error signal having the effect that the transceiver no longer acts actively on the data bus.

2. A transceiver for a serial data bus, in which the transceiver is connected via a transmission line (TXD) and a receiving line (RXD) to a protocol controller which manages a data bus protocol, and is coupled to the lines (2, 3) of the data bus, and in which the transceiver comprises means (1) for error management, which means comprise a timer circuit (16) which triggers an error signal (F) when the transmission line (TXD) is active for a longer period than a predetermined time interval, said error signal having the effect that the transceiver no longer acts actively on the data bus, which error signal is cancelled only when the transmission line (TXD) signalizes an inactive bus and the receiving line (RXD) signalizes an active bus.

3. A transceiver as claimed in claim 1, characterized in that the means (1) for error management switch off the error signal (F) when the transmission line (TXD) signalizes an inactive bus and the receiving line (RXD) signalizes an active bus.

4. A transceiver as claimed in claim 1 or 2, characterized in that the error signal (F) switches a bus transmission stage (5, 6) in the transceiver to the inactive state.

5. A transceiver as claimed in claim 1 or 2, characterized in that the error signal (F) is signalized to the exterior by means of an error line (ERR), particularly to an application having priority over a protocol controller.

6. A transceiver as claimed in claim 1 or 2, characterized in that a control line is provided, whose activation resets the means (1) for error management and thus switches the error signal (F) to the inactive state.

7. A transceiver as claimed in claims 1 and 2, characterized in that the means (1) for error management comprise a flip-flop (14) which, in the set state, supplies the error signal (F).

8. A transceiver as claimed in claims 1 and 7, characterized in that the means (1) for error management comprise a first AND gate (11) whose output signal is applied to the flip-flop (14) and which sets this flip-flop when the data bus lines (2, 3) are active and when the receiving line (RXD) simultaneously signalizes an inactive bus.

9. A transceiver as claimed in claims 2 and 7, characterized in that the timer circuit (16) in the means (1) for error management set the flip-flop (14) when the transmission line (TXD) is active for a longer period than a predetermined time interval.

10. A transceiver as claimed in claims 1, 2 and 7, characterized in that a second AND gate (17) is provided whose inputs receive the reception signal (RXD) and the transmission signal (TXD) and which resets the flip-flop (14) and thus switches the error signal (F) to an inactive state when the transmission line (TXD) signalizes an active bus and the receiving line (RXD) signalizes an inactive bus.